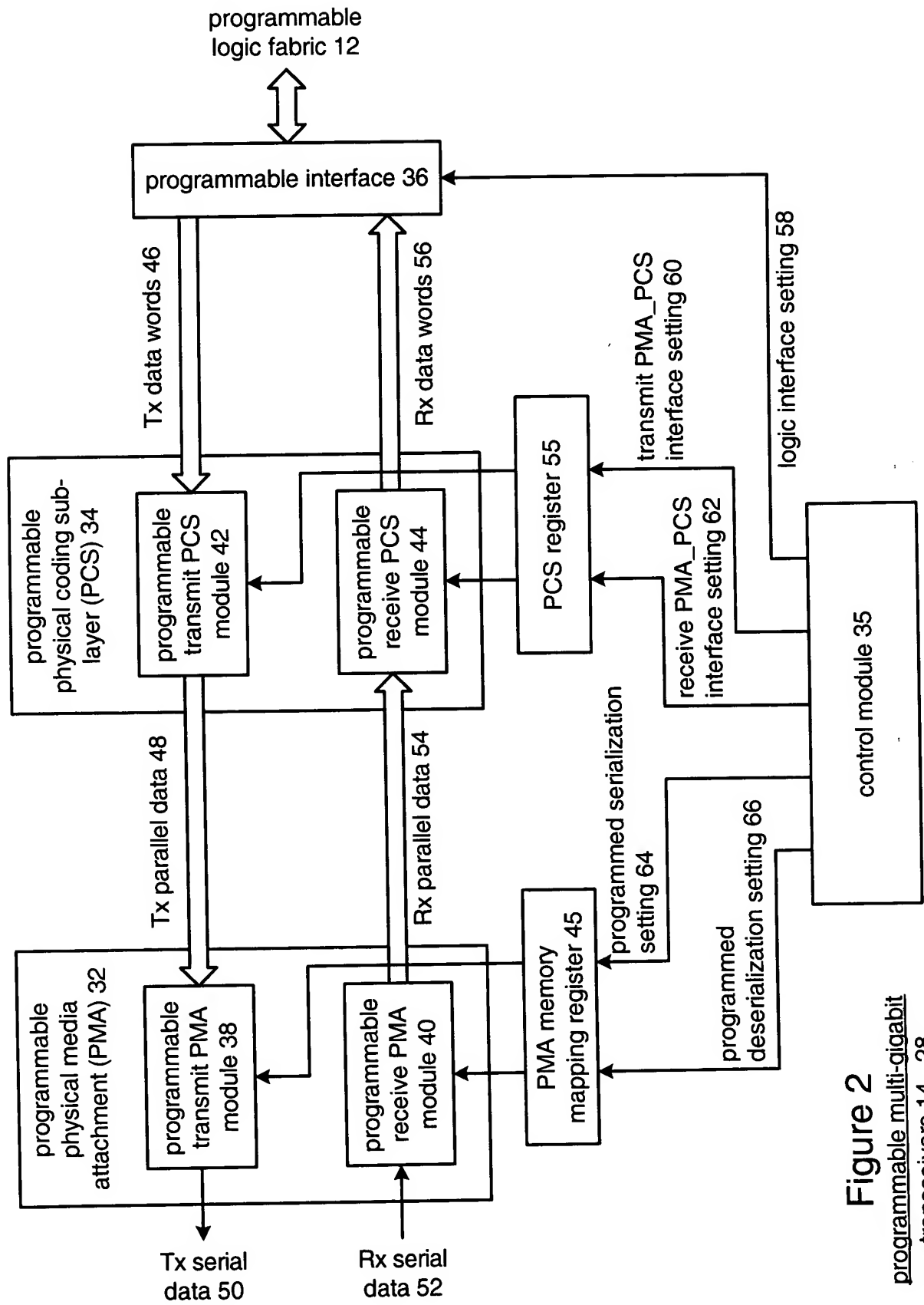
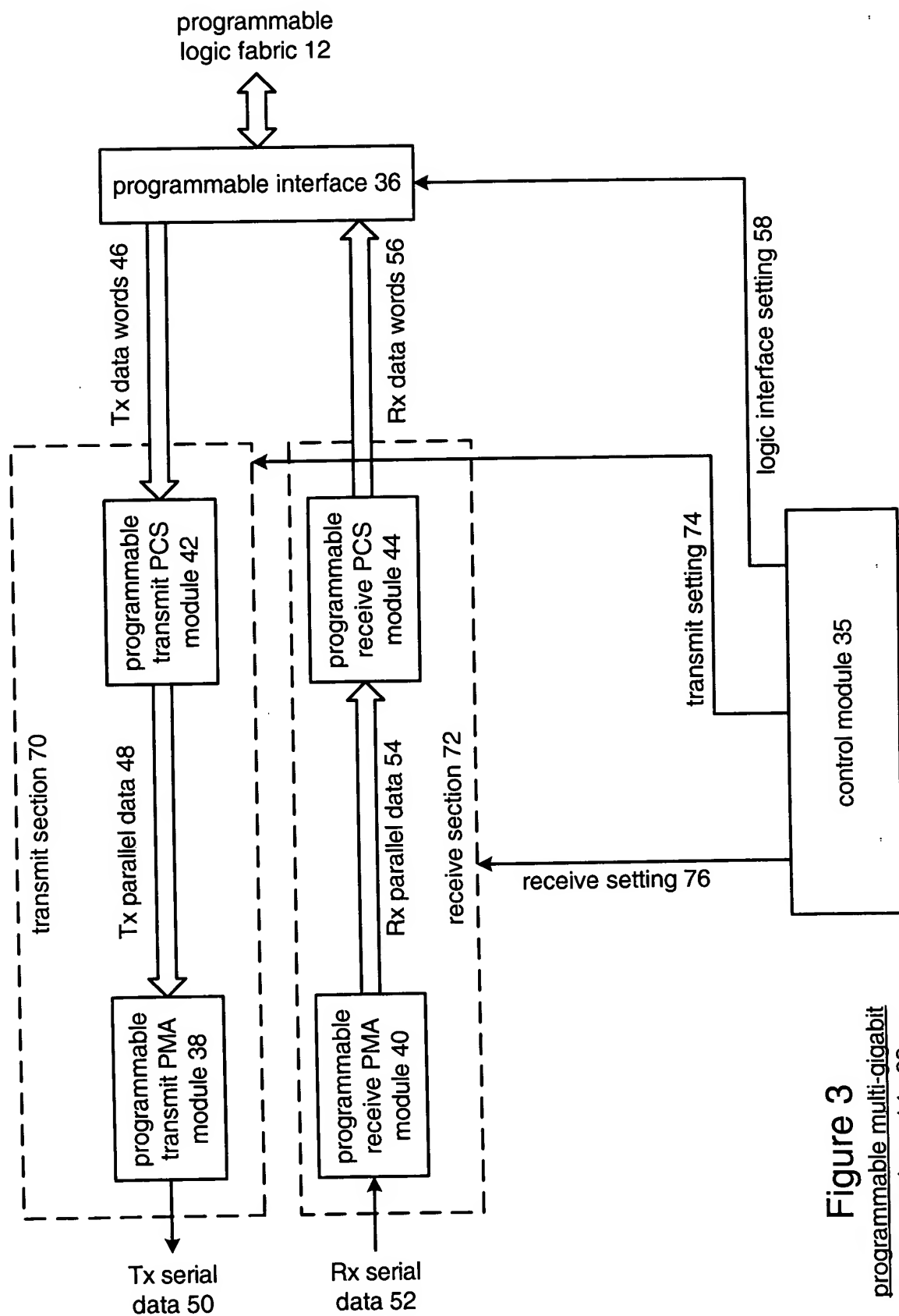


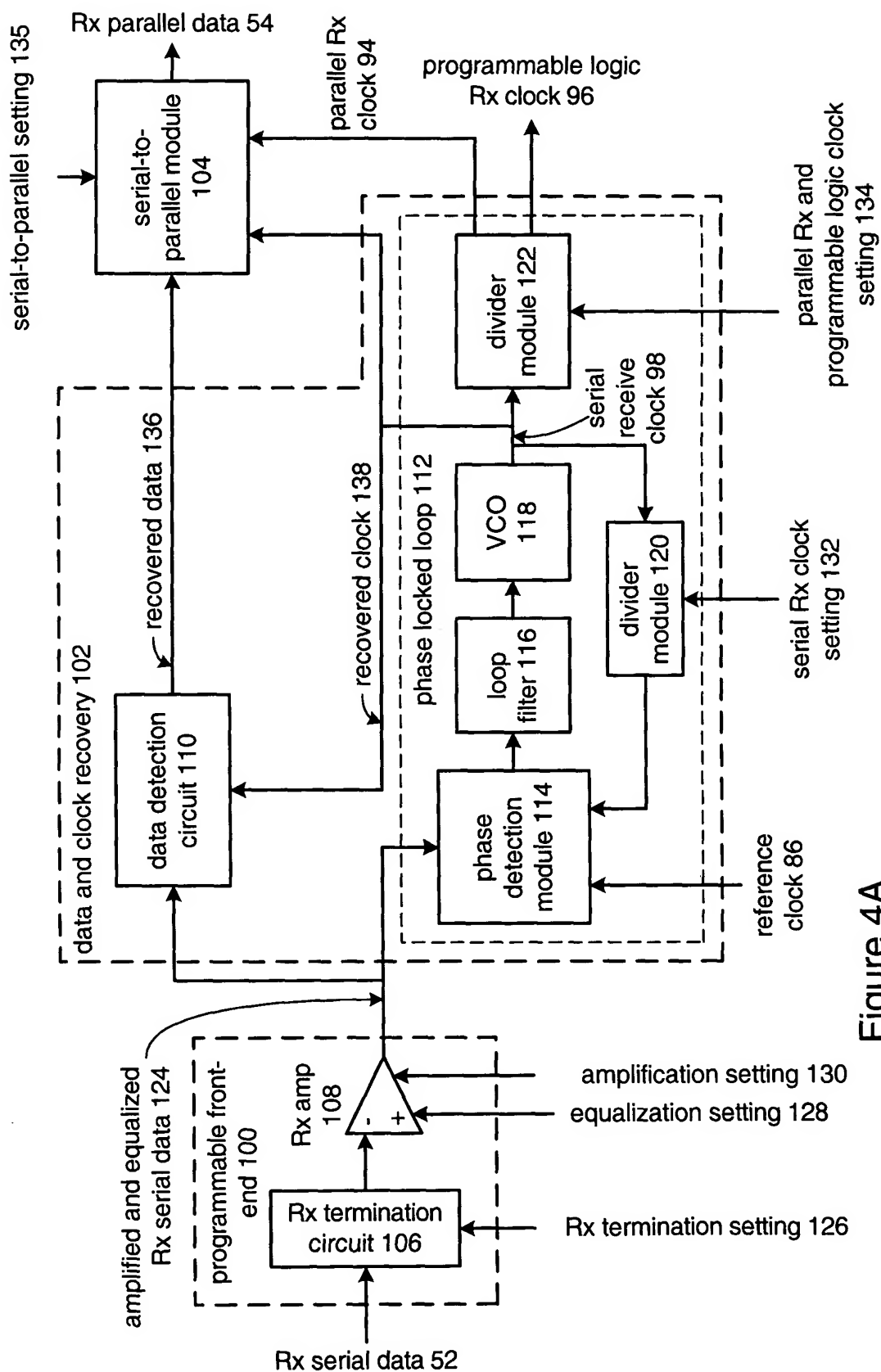
**Figure 1**  
programmable  
logic device 10



**Figure 2**  
programmable multi-gigabit  
transceivers 14 - 28

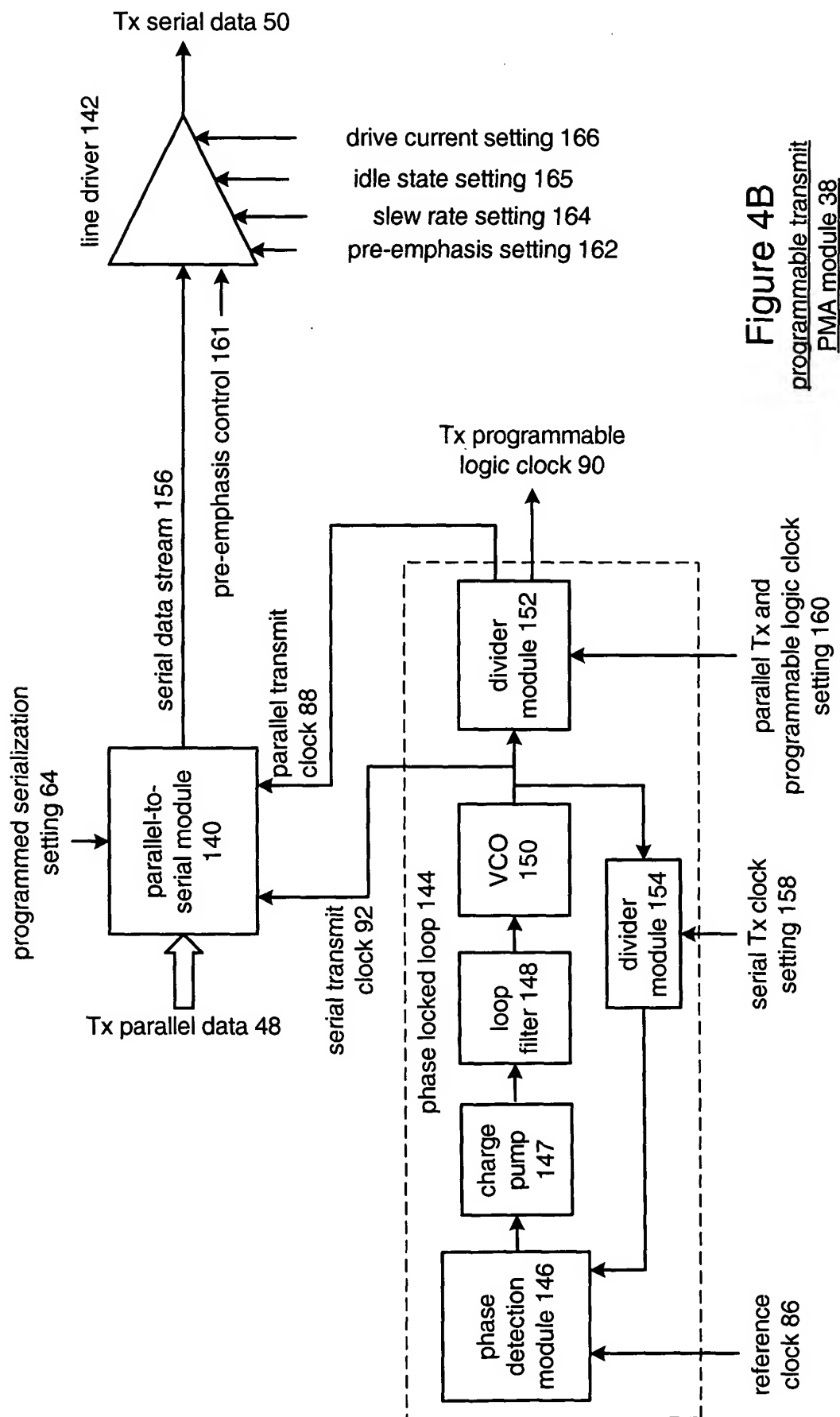


**Figure 3**  
programmable multi-gigabit  
transceivers 14 - 28



**Figure 4A**

programmable receive  
PMA module 40



**Figure 4B**  
programmable transmit  
PMA module 38

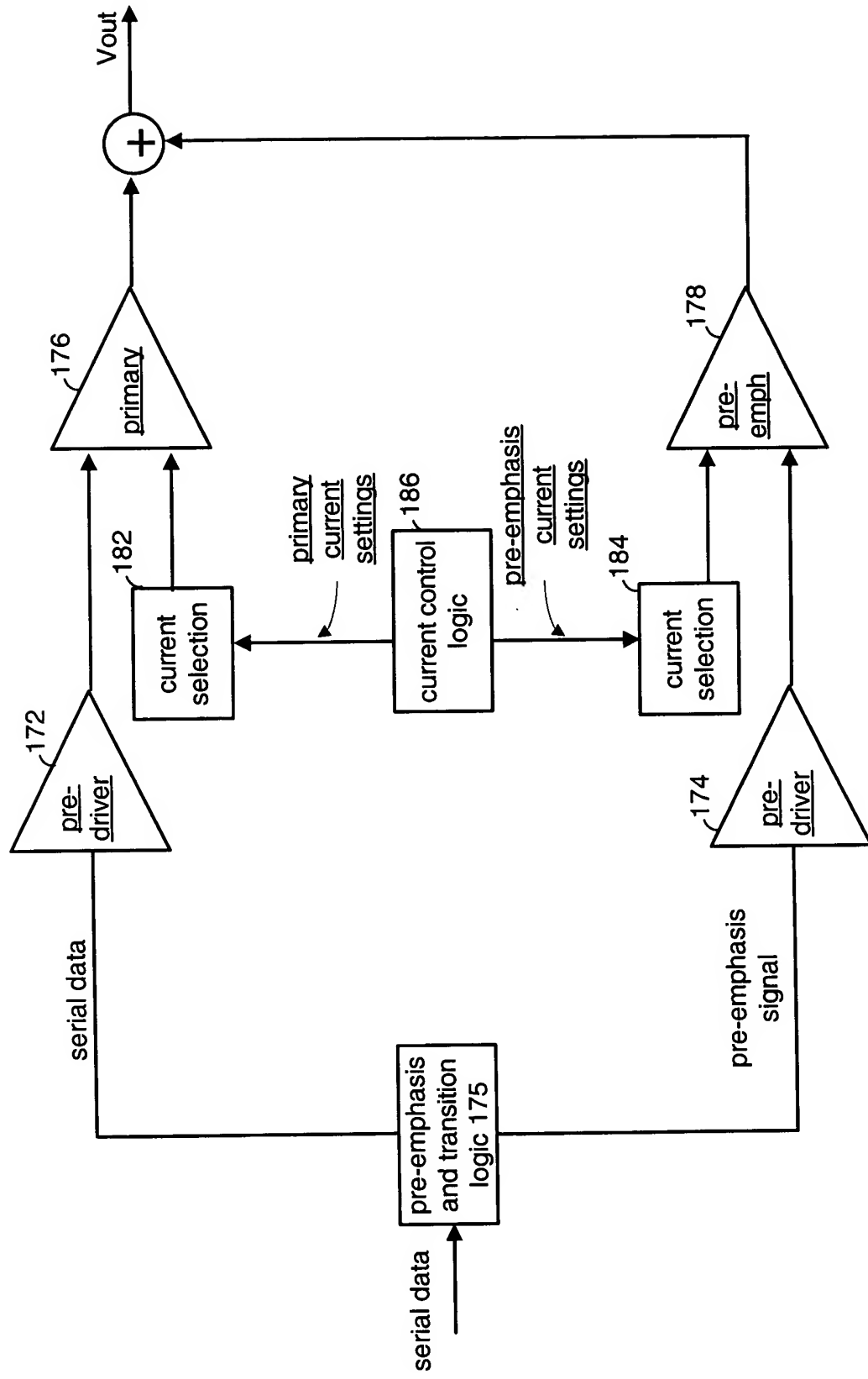


Figure 5 Tx line driver 170

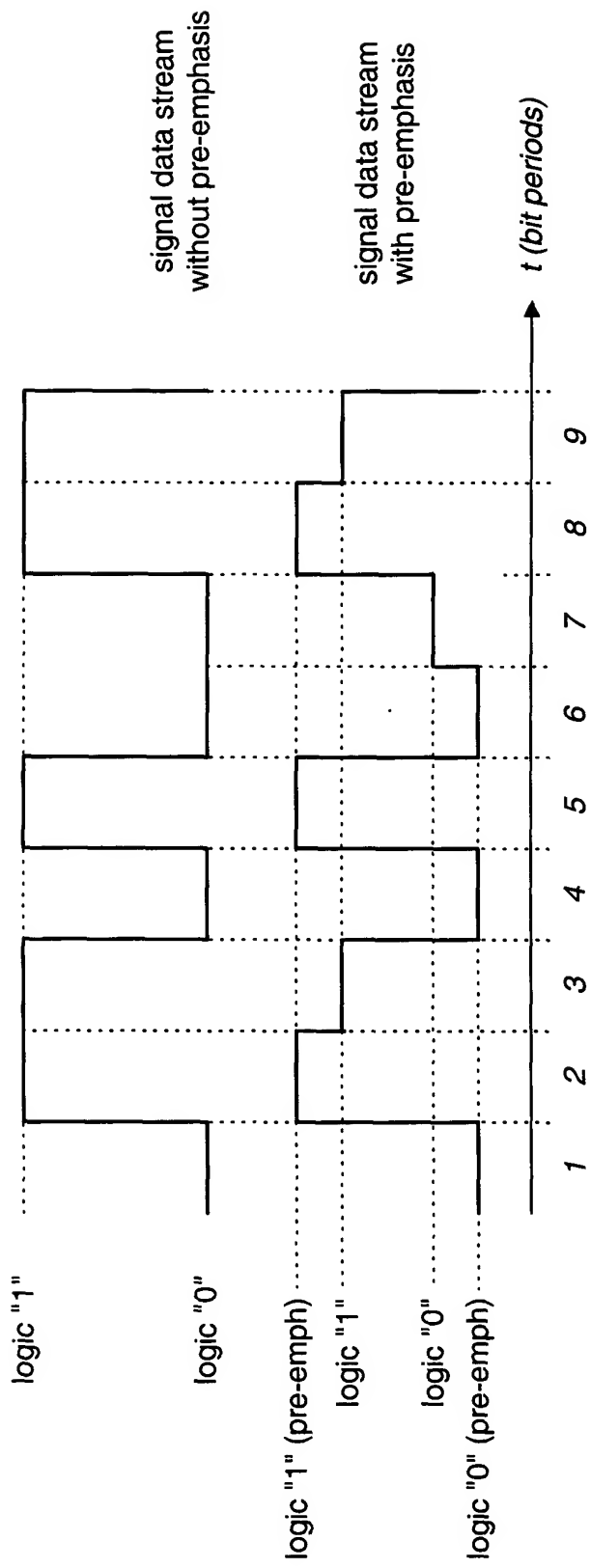


Figure 6 signal diagrams

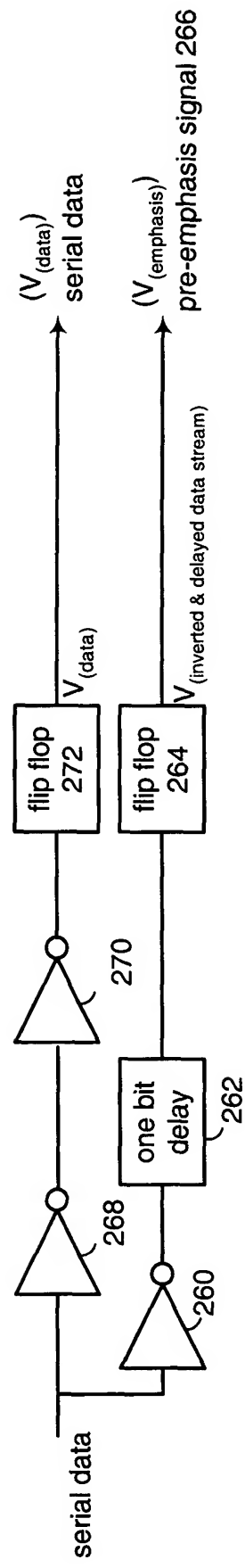


Figure 9 pre-emphasis and transition logic 175

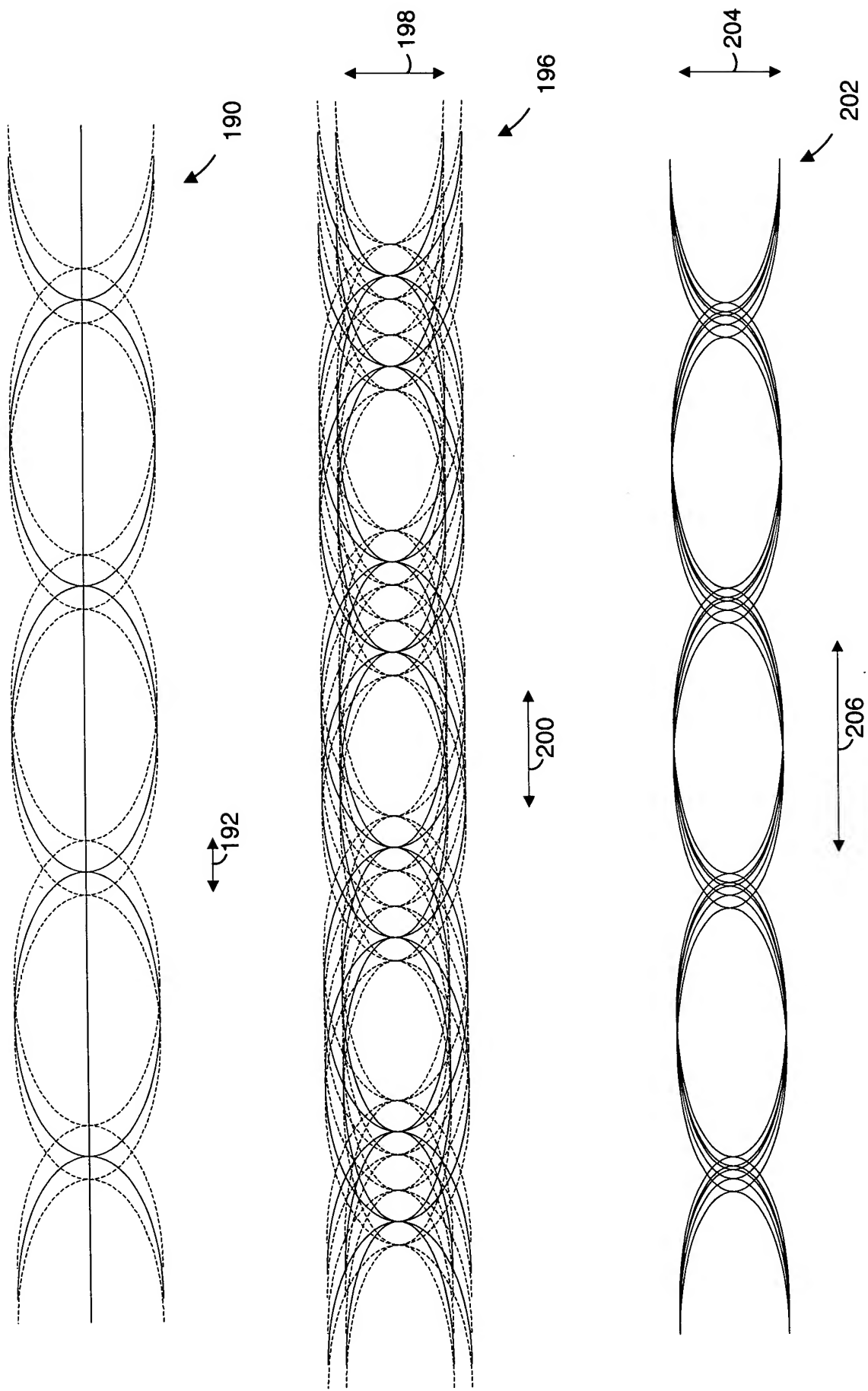
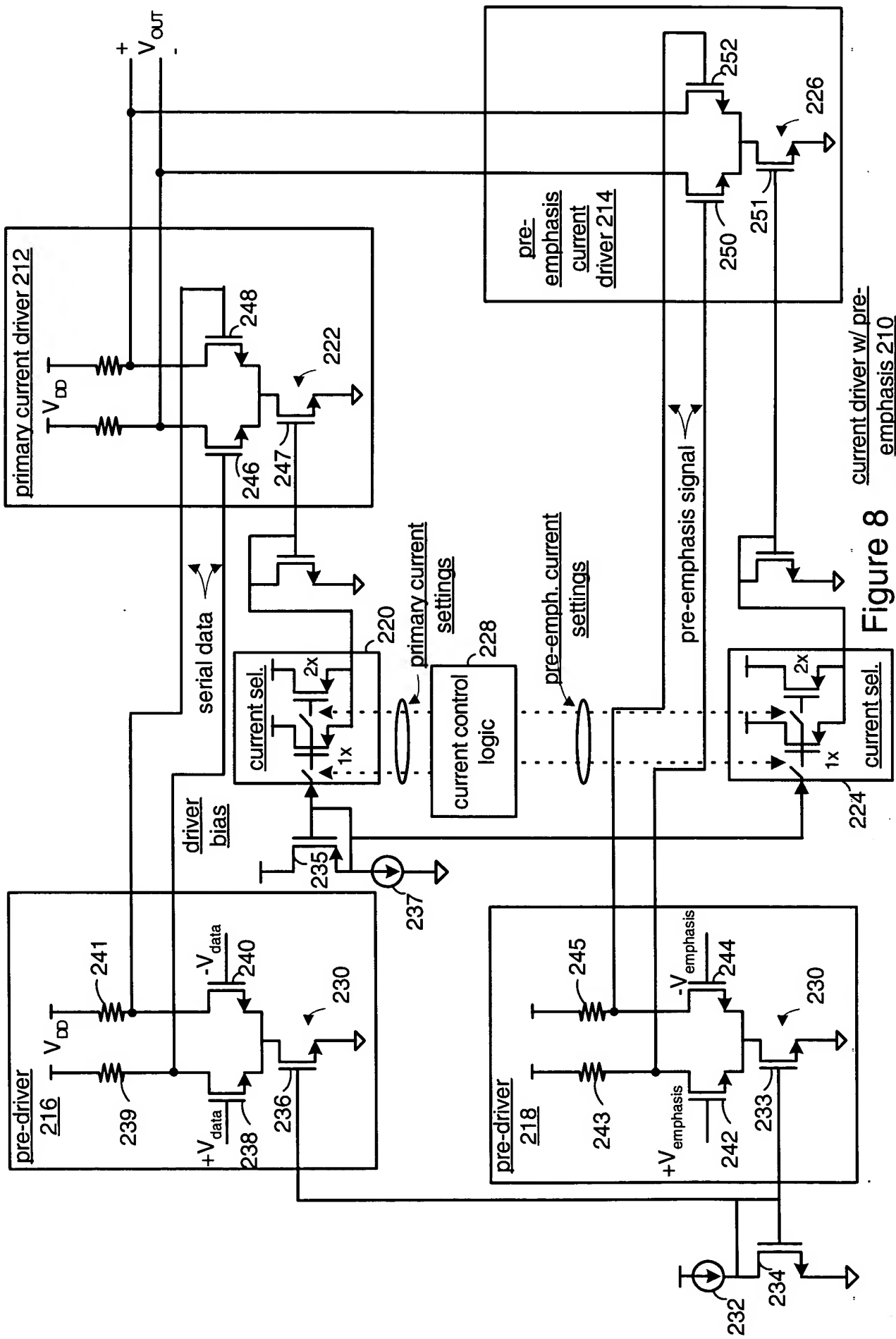


Figure 7 "eye pattern"





	x	y	n	n	y	n	n	y	n	pre-emphasis
0	1	1	0	0	1	0	0	1	1	serial data
x	1	1	0	0	1	0	1	1	0	inverted and delayed serial data (pre-emphasis signal)

Figure 10A truth table for transitions to  
logic one

	x	y	n	y	y	y	n	y	n	pre-emphasis
0	1	0	0	1	0	0	0	1	1	serial data
x	1	0	0	1	0	0	1	1	0	inverted and delayed serial data (pre-emphasis signal)

Figure 10B truth table for all transitions

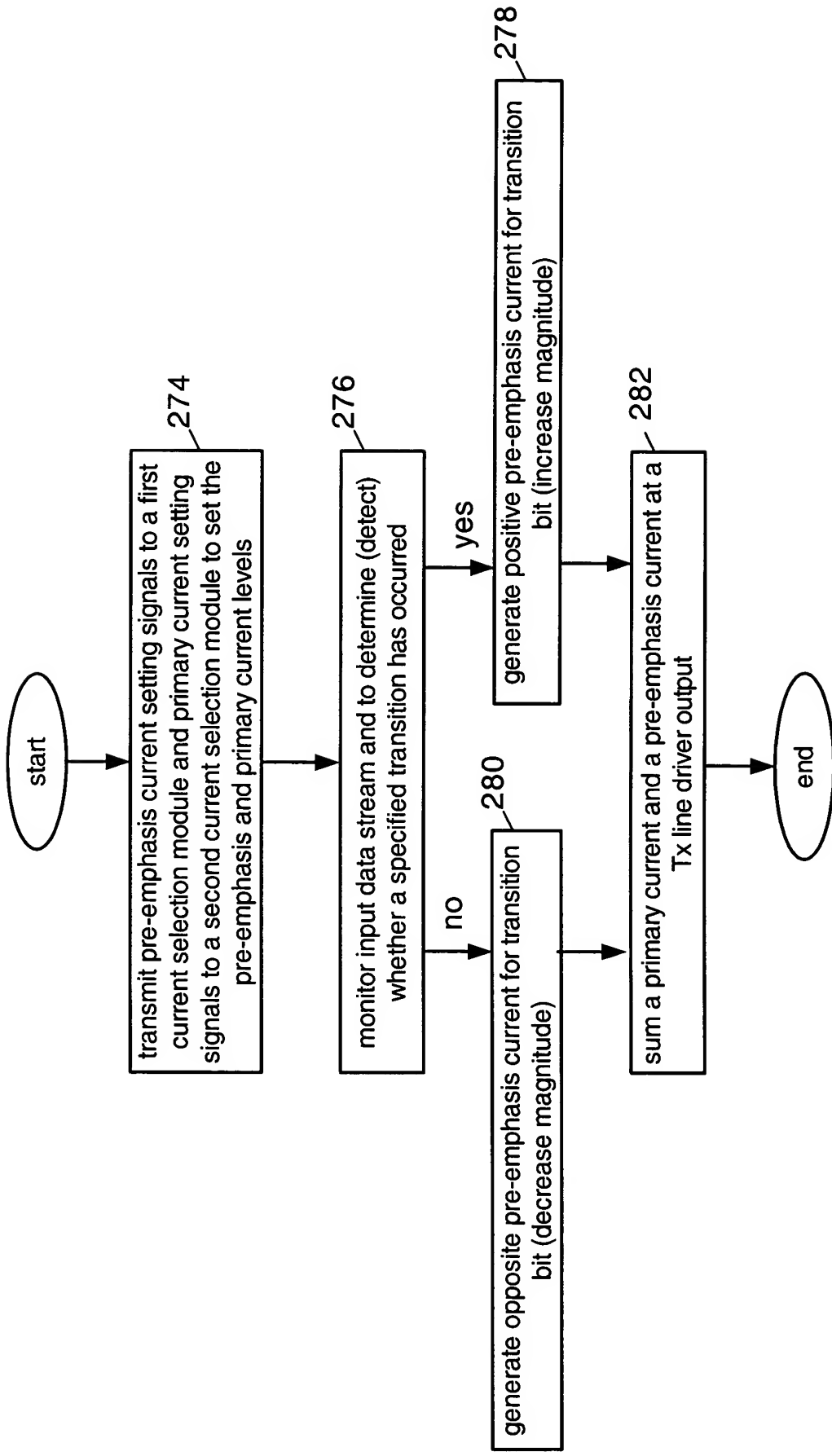


Figure 11    method for generating  
pre-emphasis